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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/756,122	01/13/2004	Wai-Fan Yau	AMAT/2592.C7/DSM/LOW K/JW	4554

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EXAMINER	
MALDONADO, JULIO J	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 10/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/756,122	YAU ET AL.	
	Examiner	Art Unit	
	Julio J. Maldonado	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-13,15-18 and 21-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-13, 15-18 and 21-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The rejection as set forth in the office action mailed on 5/12/2006 is withdrawn in view of applicants' argument in regards to claims 15-18 and 21-28, filed on 6/20/2006.

2. The indicated allowability of claim 22 is withdrawn in view of the newly discovered reference(s) to Chen to U.S. 5,970,376. Rejections based on the newly cited reference(s) follow.

3. Claims 11-13, 15-18 and 21-28 are pending in the application.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chiang et al. (U.S. 5,817,572) in view of Sugahara et al. (U.S. 5,989,998).

Chiang et al. (Figs.15-25) teach a method of forming interconnect structures including providing a substrate (320) having a contact (321) formed therein; depositing a first dielectric layer (322) on said substrate; forming an etch stop layer (323) on said first dielectric layer (322); forming a second dielectric layer (350) on said etch stop layer (323); forming a photoresist layer (352) on said second dielectric layer (350); and using said photoresist layer to form a contact hole (351) in said second dielectric layer (350), wherein said first dielectric layer (322) and said second dielectric layer (350) may include any suitable dielectric material or materials including silicon dioxide, silicon

nitride, silicon oxynitride, phosphosilicate glass, borophosphosilicate glass, fluoropolymer, parylene, polyimide, any suitable spin-on glass, or any suitable spin-on polymer, and further forming a third dielectric layer (395) over said second dielectric layer (column 13, line 27 – column 16, line 9).

Chiang et al. fail to disclose using a low dielectric constant material. However, parylene, polyimide, for example, are known low dielectric constant materials. Therefore, Chiang et al. teach upon the claimed invention.

Chiang et al. fail to teach wherein the low dielectric constant material is a an oxidized organosilane layer, wherein said organosilane layer is deposited in a plasma enhanced process from a mixture comprising an organosilane compound and an oxidizing gas and wherein the carbon content of the low dielectric constant oxidized organosilane layer is form 1% to 50% by atomic weight.

However, Sugahara et al. (Figs.3a-d) teach a method of depositing on a substrate (200) a plurality of layers (202-204), wherein one or more of the layers (202, 204) is a low dielectric constant oxidized organosilane layer comprising carbon, wherein the low dielectric constant oxidized organosilane layer is deposited in a plasma enhanced process from a mixture comprising an organosilane compound an oxidizing gas, wherein said organosilane compound is selected from a phenylsilane group or a vinylsilane group; and etching said one or more of said layers in a patterning process, wherein the carbon content of said oxidized organosilane layer is, for example, 25.7% (first embodiment, chemical formula 2) or 22.2% (ninth embodiment, chemical formula

15) (Sugahara et al., column 7, line 66 – column 8, line 8, line 34, column 8, line 58 – column 11, line 53 and column 18, line 25 – column 21, line 53).

Sugahara et al. fail to expressly teach wherein said oxidized organosilane layer has a carbon content from 1% to 50%. However, in the case where the claimed ranges "overlap or lie inside ranges disclosed by the prior art" a prima facie case of obviousness exists. MPEP 2144.05. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the dielectric layer with the carbon concentration disclosed in the teachings of Sugahara et al. to arrive at the claimed invention.

It would also have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Chiang et al. and Sugahara et al. to enable forming a low dielectric layer in Chiang et al. as taught by Sugahara et al. for the further advantage of forming a film with improved film formability and cost efficiency (Sugahara et al., column 3, lines 25 – 30) and because one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternative suitable methods of forming the disclosed dielectric layer in Chiang et al. and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

6. Claims 15-18, 21 and 23-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chiang et al. (U.S. 5,817,572) in view of Shu et al. (Patent Application, 09/019,900).

In reference to claims 15-18, 23, 24, 26-28, Chiang et al. (Figs.15-25) teach a method of forming interconnect structures including providing a substrate (320) having a contact (321) formed therein; depositing a first dielectric layer (322) on said substrate; forming an etch stop layer (323) made of silicon nitride on said first dielectric layer (322); forming a second dielectric layer (350) on said etch stop layer (323); forming a second etch stop layer (390) made of silicon nitride; forming a photoresist layer (352) on said second dielectric layer (350); and using said photoresist layer to form a contact hole (351) in said second dielectric layer (350), wherein said first dielectric layer (322) and said second dielectric layer (350) may include any suitable dielectric material or materials including silicon dioxide, silicon nitride, silicon oxynitride, phosphosilicate glass, borophosphosilicate glass, fluoropolymer, parylene, polyimide, any suitable spin-on glass, or any suitable spin-on polymer, and further forming a third dielectric layer (395) over said second dielectric layer (column 13, line 27 – column 16, line 9).

Chiang et al. fail to disclose forming the second dielectric layer using a low dielectric constant material. However, parylene, polyimide, for example, are known low dielectric constant materials. Therefore, Chiang et al. teach upon the claimed invention.

Chiang et al. fail to teach wherein the low dielectric constant organosilane layer is deposited in a plasma enhanced process from a mixture comprising a methylsilane compound and an oxidizing gas, the carbon content of the low dielectric constant oxidized organosilane layer is form 1% to 50% by atomic weight.

However, Shu et al. in a related method to form interconnect structures teach forming a low-k dielectric layer over a substrate, wherein said dielectric layer is

deposited in a plasma enhanced process from a mixture comprising a reactant species or a combination of reactant species which includes carbon and silicon, such as 3-methyltrimethoxysilane, labeled methylsilane compound, and an oxidizing gas such as O_2 and H_2O_2 (page 4, lines 9 – 22). It would have been within the scope of one of ordinary skill in the art to combine the teachings of Chiang et al. and Shu et al. to enable forming the low-k dielectric layers of Chiang et al. according to the teachings of Shu et al. because one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternative suitable methods of forming the second dielectric layer of Chiang et al. and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

The combination of Chiang et al. and Shu et al. fail to disclose wherein the carbon content of the low dielectric constant oxidized organosilane layer is form 1% to 50% by atomic weight. However, the same material would be treated in the same manner and therefore the recited results would be obtained.

In reference to claims 21 and 25, the combined teachings of Chiang et al. and Shu et al. fail to disclose wherein the methylsilane compound is methyl silane (CH_3SiH_3). However, Shu et al. teach wherein said dielectric layer is deposited in a plasma enhanced process from a mixture comprising a reactant species or a combination of reactant species which includes carbon and silicon, and an oxidizing gas such as O_2 and H_2O_2 (Shu et al., page 4, lines 9 – 22). The combination of Chiang et al. and Shu et al. further teach that conventional materials in the art to form oxide layers include methyl silane (CH_3SiH_3) (Shu et al., pate 3, line 25 – page 4, line 1). Therefore,

since methyl silane (CH_3SiH_3) is a conventional material used in the fabrication of oxide layers and the prior art of record is open to form a dielectric layer from a mixture comprising a reactant species or a combination of reactant species which includes carbon and silicon, one of ordinary skill in the art at the time the invention was made would have been envisioned to use said methyl silane to form said dielectric layer.

7. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chiang et al. (U.S. 5,817,572) in view of Shu et al. (Patent Application, 09/019,900) as applied to claims 15-18, 21 and 23-28 above, and further in view of Chen (U.S. 5,970,376).

The combination of Chiang et al. Shu et al. substantially teach the claimed invention but fail to disclose etching the low dielectric constant oxidized organosilane layer using fluorine, carbon, and oxygen ions. However, Chen (Figs.4-7) in a related method to form interconnect structures teaches the steps of forming a low dielectric layer (32) over a substrate (30), wherein said dielectric layer has the general formula R_1-$Si(OR_2)_3$, wherein R_1 is hydrogen and R_2 is CH_3; and etching the low dielectric layer (32) using fluorine, carbon, and oxygen ions (Chen, column 4, line 66 – column 5, line 12, column 5, lines 34 – 56, column 7, lines 25 – 42, and column 8, lines 40 – 48). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Chiang et al. and Shu et al. with Chen to enable etching the dielectric layer of Chiang et al. and Shu et al. according to the teachings of Chen for the further advantage of forming vias with attenuated lateral etching of said vias (Chen, column 4, lines 39 – 63).

Response to Arguments

8. Applicant's arguments filed 6/20/2006 have been fully considered but they are not persuasive.

Applicants argue, "...combining Chiang et al. and Sugahara et al. to replace the spin on glass layer in the lists of dielectric materials for layer 322 and 350 in Chiang et al. with the oxidized organosilane layer of Sugahara et al. does not provide or suggest all of the elements of claim 11, as claim 11 recites a method that includes depositing a plurality of layers including both a parylene, FSG, or silicon oxide layer and an oxidized organosilane layer. While Chiang et al. provides extensive lists of materials for the dielectric layers 322 and 350, Chiang et al. does not teach or suggest using a parylene, FSG, or silicon oxide layer for one of the dielectric layer and a different layer, such as an organic spin on glass layer or an oxidized organosilane layer, for the other dielectric layer...". In response to this argument, one of ordinary skill in the art at the time the invention was made would have been led to use different combination of the list of materials for layers 322 and 350 in Chiang et al. because there is no disclosure in Chiang et al. teaching away from an embodiment including different combinations of the materials for layers 322 and 350. Furthermore, one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternative suitable methods of forming the disclosed dielectric layer in Chiang et al. and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

9. Applicant's arguments with respect to claims 15-18 and 21-28 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

10. Applicants are encouraged, where appropriate, to check Patent Application Information Retrieval (PAIR) (http://portal.uspto.gov/external/portal/pair) which provides applicants direct secure access to their own patent application status information, as well as to general patent information publicly available.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Julio J. Maldonado whose telephone number is (571) 272-1864. The examiner can normally be reached on Monday through Friday.

12. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith, can be reached on (571) 272-1907. The fax number for this group is 571-273-8300. Updates can be found at http://www.uspto.gov/web/info/2800.htm.

Julio J. Maldonado
Patent Examiner
Art Unit 2823

Julio J. Maldonado
August 21, 2006

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